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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/891,129	06/26/2001	Akira Nishiyama	210313US2SRD	1717

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EXAMINER	
MAI, ANH D	

ART UNIT	PAPER NUMBER
2814	

DATE MAILED: 01/14/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/891,129	Applicant(s) NISHIYAMA ET AL.
	Examiner Anh D. Mai	Art Unit 2814

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *31 October 2002* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-4,6-9 and 12-26* is/are pending in the application.

4a) Of the above claim(s) *14 and 15* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4,6-9,12,13 and 16-26* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☒ The proposed drawing correction filed on *31 October 2002* is: a)☒ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 8 .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Amendment

1. Amendment filed October 31, 2002 has been entered as Paper No. 9. Claims 5, 10 and 11 have been canceled. Claims 1, 3, 4, 7, 9 and 12 have been amended. Claims 16-26 have been added. Claims 1-4, 6-9 and 12-26 are pending. Claims 14 and 15 have been withdrawn.

Drawings

2. The corrected or substitute drawings were received on October 31, 2002. These drawings are acceptable.

Claim Rejections - 35 USC § 103

The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

3. Claims 1-4, 7-9, 12 and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wallace et al. (U.S. Patent No. 6,291,867) (cited previously).

With respect to claim 1, Wallace teaches a semiconductor device substantially as claimed including:

a semiconductor substrate (20); and

a circuit element using an insulating film (36) formed in the semiconductor substrate (20), the insulating film (36) containing a silicon compound containing at least one element selected from the group consisting of oxygen and nitrogen, and a metal compound containing a metal other than silicon and at least one element selected from the group consisting of oxygen and nitrogen, the insulating film (36) further comprising crystals. (See Fig. 9).

Thus, Wallace is shown to teach all the features of the claim with the exception of explicitly disclosing the particle diameter of the crystals.

However, since the crystallizing temperature of Wallace is similar to that of the present invention, the nano-crystals grains formed within the insulating film (36) of Wallace would have a similar diameter as claimed, similar process similar result.

With respect to claim 2, the silicon compound of Wallace is a compound selected from the group consisting of a silicon oxide, a silicon nitride and a silicon oxynitride. (col. 3, ll. 10-12).

With respect to claim 3, the crystal of Wallace are made of the metal compound.

With respect to claim 4, the nano-crystal compound of Wallace is made of an oxide, a nitride or an oxynitride of metal, thus, other than silicon.

With respect to claim 7, the semiconductor device of Wallace further includes an oxynitride film (30) formed between the semiconductor substrate (20) and the insulating film (36). (See Fig. 5, col. 5, ll. 38-49).

With respect to claim 8, the metal other than silicon is at least one of metal selected from the group consisting of Zr, Hf.

With respect to claim 9, the circuit element of Wallace is a MOSFET, thus, the insulating film (36) is a gate insulating film of the MOSFET.

With respect to claim 12, since the crystals are randomly formed in the insulating film (36) of Wallace, therefore, a part of a periphery of at least one of the crystals should positioned at a distance of 0.7 nm from the interface.

With respect to claim 13, the insulating film (36) of Wallace is a mixed film containing silicon compound and metal compound.

4. Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over Wallace '867 as applied to claim 1 above, and further in view of Hsieh et al. (U.S. Patent No. 4,432,035) (cited previously).

Wallace teaches the dielectric layer may be made substantially thicker than a conventional gate dielectric with equivalent field effect. (See Col. 2, lines 30-47).

Thus, Wallace is shown to teach all the features of the claim with the exception of explicitly disclosing the thickness of the ~~if the~~ insulating layer (36).

However, Hsieh teaches a high dielectric constant and low leakage dielectric material is formed to a thickness that overlaps the claimed range. (See Abstract).

Therefore, it would have been obvious to one having ordinary skill in the art at the time of invention to form the insulating film (36) of Wallace to the thickness as taught by Hsieh to form a high dielectric constant layer for the MOSFET.

5. Claims 16-19 and 21-25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wallace '867 in view of the Background of the Invention.

With respect to claim 16, Wallace teaches a semiconductor device substantially as claimed including:

a semiconductor substrate (20); and

a gate insulating film (36) formed in the semiconductor substrate (20), the gate insulating film (36) containing a silicon compound containing at least one element selected from the group consisting of oxygen and nitrogen, and a metal compound containing a metal other than silicon and at least one element selected from the group consisting of oxygen and nitrogen, the insulating film (36) further comprising crystals; and

a gate electrode (38) formed on the gate insulating film (36). (See Fig. 9).

Thus, Wallace is shown to teach all the features of the claim with the exception of explicitly disclosing the formation of source and drain regions and the particle diameter of the crystals.

However, as shown in the Background of the Invention, Wallace discloses the formation of source and drain regions (140/160) of a well known field effect transistor. (See Fig. 1).

Therefore, it would have been obvious to one having ordinary skill in the art at the time of invention to further includes source and drain regions on the sides of the gate structure of Wallace as taught by the Background of the Invention to complete the field effect transistor.

Further, since the crystallizing temperature of Wallace is similar to that of the present invention, the nano-crystals grains formed within the insulating film (36) of Wallace would have a similar diameter as claimed, similar process similar result.

With respect to claim 17, the silicon compound of Wallace is a compound selected from the group consisting of a silicon oxide, a silicon nitride and a silicon oxynitride. (col. 3, ll. 10-12).

With respect to claim 18, the crystals of Wallace are made of the metal compound.

With respect to claim 19, the nano-crystal compound of Wallace is made of an oxide, a nitride or an oxynitride of metal, thus, other than silicon.

With respect to claim 21, the semiconductor device of Wallace further includes an oxynitride film (30) formed between the semiconductor substrate (20) and the insulating film (36). (See Fig. 5, col. 5, ll. 38-49).

With respect to claim 22, the metal other than silicon is at least one of metal selected from the group consisting of Zr, Hf.

With respect to claim 23, since the crystals are randomly formed in the insulating film (36) of Wallace, therefore, a part of a periphery of at least one of the crystals should positioned at a distance of 0.7 nm from the interface.

With respect to claim 24, the insulating film (36) of Wallace is a mixed film containing silicon compound and metal compound.

With respect to claim 25, the gate electrode (38) of Wallace comprises polycrystalline silicon layer.

6. Claim 20 is rejected under 35 U.S.C. 103(a) as being unpatentable over Wallace '867 as applied to claim 16 above, and further in view of Hsieh '035 (cited previously).

Wallace teaches the dielectric layer may be made substantially thicker than a conventional gate dielectric with equivalent field effect. (See Col. 2, lines 30-47).

Thus, Wallace is shown to teach all the features of the claim with the exception of explicitly disclosing the thickness of the if the insulating layer (36).

However, Hsieh teaches a high dielectric constant and low leakage dielectric material is formed to a thickness that overlaps the claimed range. (See Abstract).

Therefore, it would have been obvious to one having ordinary skill in the art at the time of invention to form the insulating film (36) of Wallace to the thickness as taught by Hsieh to form a high dielectric constant layer for the MOSFET.

7. Claim 26 is rejected under 35 U.S.C. 103(a) as being unpatentable over Wallace '867 as applied to claim 16 above, and further in view of Bai et al. (U.S. Patent No. 5,818,092).

Wallace teaches all the features of the claim with the exception of further includes silicide layers formed on the source and drain regions (140/160).

However, Bai teaches field effect transistor (100) formed on a semiconductor substrate (101) further includes silicide layer (114) formed on the source and drain regions (110).

Therefore, it would have been obvious to one having ordinary skill in the art at the time of invention to further includes silicide layers on the source and drain regions (140/160) of Wallace as taught by Bai to reduce sheet resistance. (See col. 1, lines 13-22).

Response to Arguments

8. Applicant's arguments filed October 31, 2002 have been fully considered but they are not persuasive.

With respect to the nano-crystals applicant argues: "In order to obtain nano-crystals having a diameter within a range of between 1 nm and 10 nm, the insulating film **must essentially be an oxide**".

However, contrary to the applicant's assertion, the limitation of the claims includes: "the gate insulating film (36) containing a silicon compound containing at least one element selected from the group consisting of **oxygen and nitrogen**" and "said silicon compound is a compound selected from the group consisting of a silicon oxide, a silicon nitride and a silicon oxynitride". Therefore, the formation of the nano-crystals having the diameter as claimed do not exclusive of oxide.

Further, the specification fails to support the applicant's assertion.

Conclusion

9. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

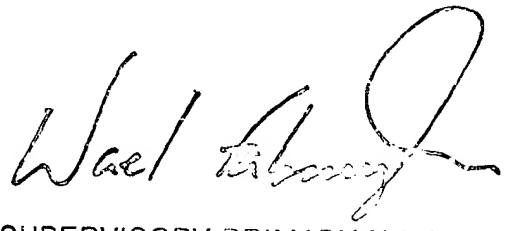
A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Anh D. Mai whose telephone number is (703) 305-0575. The examiner can normally be reached on 8:30AM-5:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael Fahmy can be reached on (703) 308-4918. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 308-7722 for regular communications and (703) 308-7722 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

A.M
January 9, 2003



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